

**INFORMATION
DISCLOSURE
CITATION**
PTO-1449

Customer Number:
26615

ATTORNEY'S DCT NO.
H1442

APPLICATION NO.
Unassigned 10/728,

APPLICANT(S)
Wiley Eugene Hill et al.

FILING DATE
December 8, 2003

GROUP
2818
Unassigned

910

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
<i>TH</i>	4,996,574	02-26-91	Shirasaki	357	23.7	06-30-89

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>TH</i>	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
<i>TH</i>	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.
<i>TH</i>	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
<i>TH</i>	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.
<i>TH</i>	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
<i>TH</i>	Co-pending U.S. Application Serial No. 10/638,334, filed August 12, 2003, entitled: "Systems and Methods for Forming Dense N-Channel and P-Channel Fins Using Shadow Implantation," 16 page specification, 18 sheets of drawings.
<i>TH</i>	Co-pending U.S. Application Serial No. 10/429,697, filed May 6, 2003, entitled: "FinFET-Based SRAM Cell," 16 page specification, 12 sheets of drawings.

EXAMINER	DATE CONSIDERED
<i>TH TH HO</i>	<i>Oct 04</i>

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).